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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO-0037-VA	5927

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/605,293	Applicant(s) CHAPEK, DAVID L.	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 12 line 16 includes the limitation of the series of sources and drains being formed **in** the plurality of die. Line 17 includes the limitation of the series of sources and drains being formed **on** the substrate. The die are formed of the substrate as claimed in lines 2-3. It is indefinite how the sources and drain can be formed in the die and on the substrate as the die and substrate are the same structure.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Henley et al. (U.S. Patent No. 6083324).

Applicant's admitted prior art discloses on page 1 lines 12-16 a semiconductor substrate, a layer of silicon dioxide on the substrate, and a layer of polycrystalline silicon

formed on the silicon dioxide, the polycrystalline silicon having a smooth morphology. The admitted prior art discloses the layer of silicon dioxide having been doped with hydrogen ions. The semiconductor substrate is considered as a bottom portion of the silicon dioxide layer with the remaining silicon dioxide layer as the silicon dioxide layer upon the substrate. Though the admitted prior art does not explicitly state a layer of polysilicon is on the silicon dioxide it is implicitly understood that the polysilicon is formed seeing that the admitted prior art discusses performing the hydrogen doping of the silicon dioxide so as to provide a thinner, smoother polysilicon film deposited on the silicon dioxide. The admitted prior art of lines 16-22 does not teach the layer of silicon dioxide being free of sputtered metal contaminants as the Kaufman ion source causes metal contaminants in the layer. The admitted prior art teaches the metal contaminants being produced from metal sputtering off a metal grid in the Kaufman ion source apparatus and that as device sizes decrease the effect of the damage from the metal contaminants increases.

Henley et al. teach a plasma immersion ion implantation apparatus for implanting hydrogen ions into semiconductors. It is noted that plasma source ion implantation (PSII or PSI) and plasma immersion ion implantation (PIII) are interchangeable terms for the same plasma treatment. Henley et al. teach that their implantation method can be used on SOI (silicon-on-insulator) substrates in column 2 lines 30-40 and teach implanting hydrogen ions in line 38, for example.

Applicants admitted prior art and Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been

obvious to a person of ordinary skill in the art to implant the hydrogen using the PSII technique of Henley et al. The motivation for doing so is to that PIII is cost effective, easy to use, and produces less impurity metal contamination. Therefore, it would have been obvious to combine Applicant's admitted prior art with Henley et al. to obtain the invention of claim 9.

5. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of Applicant's admitted prior art with Henley et al. as applied to claim 9 above.

Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, a silicon dioxide layer formed on at least a portion of the substrate, a layer of polycrystalline silicon formed on at least a portion of the silicon dioxide layer, and a gate oxide formed on the substrate from the layer of silicon dioxide, and a source and a drain in the substrate where a gate electrode is formed on the substrate from the layer of polycrystalline silicon. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16 and Henley et al. teach using a PSII method to implant the hydrogen. Applicant's admitted prior art with Henley et al. as discussed above also teach the silicon dioxide as being free of sputtered metal contaminants. In the combination of the references, the gate oxide would be formed from the layer of silicon

dioxide having hydrogen ions implanted therein and the layer of polycrystalline silicon formed on the layer of silicon dioxide would have a smooth morphology.

Burns et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art and Henley et al. to obtain the invention of claim 10.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate oxide, source, and drain formed on the substrate and a gate electrode for each transistor formed of the layer of polycrystalline silicon. The gate oxide for each transistor of the combination of references would be formed of the silicon dioxide having hydrogen atoms implanted therein.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in

semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs. Also, the gate electrode is a repeating series of gate electrodes for each transistor on each die formed from the layer of polycrystalline silicon.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of Applicant's admitted prior art with Henley et al. as applied to claims 9-12 above.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate 501 of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a gate oxide formed from the insulating layer, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a gate electrode 504 formed on the insulating layer. Murata et al. do not teach the substrate having hydrogen ions implanted therein or the substrate being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. Henley et al. as discussed above teach using a PSII method to implant the hydrogen. Applicant's admitted prior art with Henley et al. as discussed above also teach the silicon dioxide as being free of sputtered metal contaminants. In the combination of the references, the layer of polycrystalline silicon formed on the layer of substrate would have a smooth morphology.

Murata et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Murata et al. with Applicant's admitted prior art and Henley et al. to obtain the invention of claim 14.

Response to Arguments

7. Applicant's arguments with respect to claims 9-12 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800